

macros. WriteBack and Read/Write can be performed in the same macro within the same cycle.

## BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the present invention will become apparent from the accompanying detailed description and drawings, wherein:

*including Fig. 1A, Fig. 1B and Fig. 1C*

Fig. 1 shows exemplary embodiments of DRAM primary sense amplifiers with data storage and data write-back capability, and two amplification stages;

Fig. 2 shows an exemplary embodiment of a DRAM primary sense amplifier with data storage and data write-back capability;

Fig. 3 shows an exemplary embodiment of a DRAM secondary sense amplifier with two amplification stages;

Fig. 4 shows examples of executed operation and timing of the pipelined architecture DRAM;

*including Fig. 5A and Fig. 5B*

Fig. 5 shows waveform examples on various nodes of the pipelined architecture

DRAM; *including Fig. 6A and Fig. 6B*

Fig. 6 shows exemplary embodiments of various modular DRAM size increases;

and

Fig. 7 shows an exemplary floorplan of a two dimensional growable Read/Write/WriteBack DRAM.